REMARKS

The Applicants request reconsideration of the rejection. Claims 1-12 are pending.

The Examiner objected to claims 10 and 12 for minor informalities noted on page 2 of the Office Action. Without changing the scope of the claims, the Applicants have amended claims 10 and 12 to make the corrections suggested by the Examiner.

Claims 1-2, 4-8, and 11 were rejected under 35 U.S.C. § 102(b) as being anticipated by Hanaoka et al U.S. Patent No. 5,521,590 (Hanaoka). The Applicants traverse as follows.

Claim 1 features first means for releasing inner elements of a semiconductor device from a reset (inactive) state and putting the inner elements in an active state when a voltage attained by rectifying an AC wave received from an antenna is higher than a predetermined voltage value, wherein, in the reset state, the impedance of the semiconductor device is maintained at a low impedance state. This situation is illustrated, for example, in Figure 7 of the present application. Note "R INPUT SIGNAL" of flip-flop 64a and the corresponding "SWITCHING BEHAVIOR OF FET 9, 10", which exhibits the ON state during the reset. As shown in Figure 6,

the ON state of FETs 9, 10 add resistors 11, 12 between coil 3 and ground, thereby lowering the impedance of the semiconductor device.

In contrast, Hanaoka discloses that the impedance is high in the case of the reset state, and low in the reset release state, the exact opposite of the presently claimed invention. The Hanaoka situation is illustrated in Figure 4 of the present application. Note "R INPUT SIGNAL" and "SWITCHING BEHAVIOR OF FET 9, 10", referring to Figure 2. Figure 4 shows that the FETs 9, 10 are OFF during the reset period.

Claim 2 is dependent from claim 1, and thus inherits the patentability of claim 1. Note, further, that claim 2 recites the characteristic shown in Figure 8, in which the reset release voltage is substantially equal to the logic working guarantee voltage.

Independent claims 4-8 recite similar language respecting the low impedance state of the semiconductor device or integrated circuit element during reset. Therefore, claims 4-8 are also patentable.

Claim 11 is dependent upon claim 1, and is directed to an IC card having the RFID set forth in claim 1. Therefore, claim 11 is also patentable.

Claim 3 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hanaoka in view of Hirano et al U.S. Patent No. 6,246,624 (Hirano). Claim 3, however, is derived from claim 1 via claim 2, and thus is patentable for the same reasons that claims 1 and 2 are patentable.

Claims 9, 10, and 12 were rejected under 35 U.S.C. § 103 as unpatentable over Hanaoka in view of Beigel U.S. Patent No. 5,973,598 (Beigel). Claims 9 and 10 are both independent claims limited by requiring that, when a voltage applied to power-on-reset means is below a threshold level, the integrated circuit element is maintained at a low state (claim 9) and that a terminal of a load resistor connected to the coil is grounded (claim 10). Therefore, claims 9 and 10 are patentable for the same reason that claim 1 is patentable.

Dependent claim 12 inherits the patentability of claim 10.

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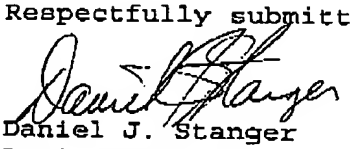
Each aspect of the rejection having been addressed, the Applicants request reconsideration of the rejection and allowance of the claims.

Respectfully submitted,



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